Registration No.: | | | | | | | | | | |

Total Number of Pages: 02 **Course: M.Tech**

Sub_Code: P1CSBC03

1st Semester Regular/Back Examination: 2023-24

SUBJECT: Advanced Computer Architecture

BRANCH(S): COMPUTER SCIENCE AND ENGG, COMPUTER SCIENCE AND TECH.

Time: 3 Hour

Max Marks: 100

Q.Code : N555

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) What do you mean by Distributed memory system?

b) A four-stage pipeline has stage delays as 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate, calculate the total time taken to process 1000 data items on this pipeline.

c) What do you mean by Spatial and Temporal locality of reference?

d) How can an interleaved memory mechanism be used to improve the processing speed of a computer system?

e) What do you mean by pipeline interlock?

f) What is a Delayed branch? How does it improve the Performance of a pipeline architecture?

g) Differentiate between Address space and Memory space.

h) A CPU generates 32-bit virtual addresses. The page size is 4kB. The processor has a TLB which can hold a total of 256 page table entries. The TLB is an 8-way set associative. Calculate the TLB tag size.

i) What are the disadvantages of using symmetric shared memory?

j) Write any two differences between Superscalar architecture and Super pipelined architecture.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Compare CISC and RISC computer architectures.

b) Name and explain the different network topologies used in interconnection network architecture.

c) An 8 kB 4-way set associative write back cache is organized as multiple blocks, each of 32-byte size. Assume that the processor generates 36 bits addresses. Calculate the total size of memory required by cache controller to store the tags for cache?

d) Distinguish between UMA and NUMA architecture.

e) What is cloud computing explain its characteristics and features?

f) What is cache coherence problem and when do you say a memory system is coherent? What are cache coherence protocols?

g) Consider the page reference string 0, 1, 3, 6, 2, 4, 5, 2, 5, 0, 3, 1, 2, 5, 4, 1, 0. The number of page frames is 4. What would be the number of page faults generated for OPTIMAL and LRU page replacement algorithms.

h) Briefly describe the V.L.I.W. processor architecture. What are the differences between superscalar processor and VLIW processor?

i) A program consists of 2500 instructions. The proportion of different kinds of instructions in the program is as follow:
Data transfer instruction 50%, arithmetic instruction 30%, and branching related instructions 20%. The cycles consumed by these types of instructions are 2, 5, and 10 respectively. What will be the execution time for a 4 GHz processor to execute your program?

j) Explain in detail about the different components of centralized shared memory architecture and distributed shared memory architecture.

k) Discuss in detail the working of set associative mapped cache with four blocks per set with relevant data. A block-set associative cache consists of a total of 64 blocks divided into 4 blocks sets. The main memory contains 4096 blocks, each consisting of 128 words.

I. How many bits are there in the main memory address?

II. How many bits are there in each of the TAG, SET, and WORD fields?

l) Discuss the various techniques available for reducing cache miss penalty. Suppose that in 1000 memory reference there are 50 misses in the first level cache and 20 misses in the second level cache. What are the various miss rates? Assume the miss penalty from the L2 cache to memory is 100 clock cycles the hit time of the L2 cache is 10 clock cycles. The hit time of L1 is 1 clock cycle and there are 2 memory references per instruction. What is the average memory access time?

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Describe Flynn's classification of computer architecture. Compare the features of Array Processor and Vector Processors. **(16)**

Q4 What is Locality of Reference and explain about Cache memory in detail. Illustrate the mapping process involved in transformation of data from main to Cache memory. A computer has a 4 GByte memory with 32 bit word sizes. Each block of memory stores 32 words. The computer has a direct-mapped cache of 64 blocks. The computer uses word level addressing. What is the address format? If we change the cache to an 8-way set associative cache, what is the new address format? **(16)**

Q5 Explain in detail about data flow computer architecture. Distinguish between static data flow computer and dynamic data flow computer. **(16)**

Q6 Explain the different classes of pipeline hazards with examples in detail. Consider a 4-stage pipeline that consists of Instruction Fetch (IF), Instruction Decode (ID), Execute (Ex) and Write Back (WB) stages. The times taken by these stages are 50 ns, 60 ns, 110 ns, and 80 ns respectively. The pipeline registers are required after every pipeline stage, and each of these pipeline register consumes 10 ns delay. What is the speed-up of the pipeline under ideal conditions compare to the corresponding non-pipelined implementation? **(16)**

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Total Number of Pages: 02 **Course: M.Tech**

Sub_Code: P1CSBC04

1st Semester Regular/Back Examination: 2023-24

SUBJECT: Advanced Data Structure and Algorithm

BRANCH(S): COMPUTER SCIENCE AND ENGG, COMPUTER SCIENCE AND TECH.

Time: 3 Hour

Max Marks: 100

Q.Code: N589

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right-hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) A two-dimensional array consisting of 8 rows and 3 columns is stored in a row major order. Compute the address of element A (4, 2). Base address is 1000 and word length is 2. Find the address of the same element in the column major representation.

b) What are the advantages in reverse polish (prefix and postfix notation) over polish (infix) notation?

c) Write the differences between spanning tree and minimum spanning tree.

d) What is Binary heap?

e) How NP-hard problems are different from NP-Complete?

f) What is a circular queue? How do you check the queue full condition?

g) Define Binomial Heap.

h) Define Splay Tree.

i) Define B-tree.

j) What are the drawbacks of AVL trees?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Write and explain Cook's theorem.

b) Determine an LCS of <1, 0, 0, 1, 0, 1, 0, 1> and <0, 1, 0, 1, 1, 0, 1, 1, 0>.

c) Solve the recurrence relation: $T(n) = 3\,T(n/4) + n$

d) Write the algorithms for PUSH, POP and change operations on stack. Using these algorithms, how do you check whether the given string is a palindrome?

e) A file contains only colons, spaces, newlines, commas and digits in the following frequency. Colon- 100, space- 605 newline- 100, comma- 705, 0- 431, 1- 242, 2- 176, 3- 59, 4 - 185, 5 - 250, 6 - 174, 7 - 199, 8 - 205, 9 - 217. Construct the Huffman code. Explain Huffman algorithm.

f) Write the algorithm to compute 0/1 Knapsack problem using dynamic programming and explain it.

g) Explain the methodology of Dynamic programming. List the applications of Dynamic programming.

h) Explain the single source shortest path problem with an example.

i) Write an algorithm for 2-3 Tree deletion and discuss its analysis.

j) Find out the inorder, preorder, postorder traversal for the binary tree representing the expression (a + b*c)/ (d – e) with the help of procedures.

k) Show step by step process for constructing binary heap using the following data 10, 12, 1, 14, 6, 5, 8, 15, 3, 9, 7, 4, 11, 13, and 2.

l) Write and explain Floyd-Warshall's algorithm.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 What is the representation of binary tree in memory? Explain in detail. Explain the B-tree with insertion and deletion operations. **(16)**

Q4 Explain three possible cases for inserting a node in the 2-3 Trees? Construct 2-3 Trees with the following data 50, 20, 60, 90, 40, 100, 10. **(16)**

Q5 Explain the relationship between class P, NP, NP-complete and NP hard problem with example of each class. **(16)**

Q6 Construct a minimum spanning tree using Kruskal's algorithm with your own example. **(16)**

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Total Number of Pages : 02 **Course: M.Tech**

Sub_Code: P1CSBC05

1st Semester Regular/Back Examination: 2023-24

SUBJECT: Advanced Operating System

BRANCH(S): CSE,CST

Time : 3 Hour

Max Marks : 100

Q.Code : N617

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions :** **(2 x 10)**

a) How Virtual memory implemented in an operating system?

b) What is the significance meaning of a cycle in Resource Allocation Graph?

c) Which algorithm used to determine the order of events?

d) Where do you find the applications of Queuing Theory?

e) What is phantom deadlock?

f) Distinguish between Physical clock and Logical clock.

g) Define orphan message.

h) Write any two main advantages of process migration.

i) Compare between network operating system and distributed operating system.

j) Define Name Space with example.

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) What are the different process migrations in distributed system?

b) What are the differences between a stateful and stateless server?

c) Describe Ricart-Agrawala's distributed mutual exclusion algorithm.

d) Name an algorithm that is able to detect 'false deadlock' for distributed deadlock detection. Show how it is detected.

e) What are partial ordering and total ordering in distributed operating system? How can partial ordering of 'happened-before' relation be converted to total ordering?

f) Explain the architecture of Distributed File system with a neat diagram.

g) Discuss the 'capability-based' implementation of Access matrix model along with its advantages.

h) How is a Remote Procedure Call performed? Show the steps in detail.

i) Identify different types of criteria for selecting a suitable load sharing algorithm.

j) What is the difference between load balancing and load sharing?

k) Identify different types of system failures.

l) What are the advantages and disadvantages of Distributed Shared Memory?

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** What is Clock synchronization? How computer clocks are implemented? What is clock drift? **(8)**

b) Define distributed Operating system. Explain different issues in distributed Operating systems. **(8)**

Q4 **a)** What different transparencies can be achieved through distributed system? What are the underlying advantages? **(8)**

b) State different types of deadlock detection algorithm in Distributed system. Explain hierarchical deadlock detection algorithms in details. **(8)**

Q5 **a)** Compare and contrast the properties of synchronous and asynchronous Byzantine agreement protocols in distributed systems. **(8)**

b) What are the two important goals of distributed file system? Explain the mechanisms for building distributed file systems. **(8)**

Q6 **a)** State the central issues in the implementation of Distributed Shared Memory (DSM). Explain various types of algorithms to implement DSM systems. **(8)**

b) Differentiated between Sender and receiver-initiated algorithm. Explain different policies of receiver-initiated algorithm with its limitations. **(8)**

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Total Number of Pages: 02 **M.Tech**
P1PGCC01

1ST Semester Regular/Back Examination: 2023-24
COMPUTATIONAL METHODS AND TECHNIQUES
BRANCH(S): ALL
Time: 3 Hour
Max Marks: 100
Q.Code: N483

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.
The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2×10)**

a) What do you mean by an Artificial Neural Network?
b) Draw a schematic for multi-layer feed forward artificial neural network.
c) Differentiate between supervised and unsupervised learning.
d) What do mean by Linguistic variables? State its significance.
e) State 2 industrial applications of Fuzzy Logic.
f) Define Cartesian product of two fuzzy sets with an example.
g) What do you mean by Hybridization of optimization techniques? Briefly explain.
h) What is a PSO algorithm? Briefly explain.
i) State a basic inequality constrained optimization problem.
j) Define a Linear Programming optimization (Simplex Method).

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Define membership function and its importance in fuzzy logic.
b) What is the generalized delta rule? Derive it. Why is this useful?
c) Determine the maximum and minimum values of the function f (x) = $12x^5 - 45x^4 + 40x^3 + 5$.
d) Find the extreme points of the function f (x_1, x_2) = ${x_1}^3 + {x_2}^3 + 2{x_1}^2 + 4{x_2}^2 + 6$.
e) Consider two given fuzzy sets.
A = {1/2, 0.3/4, 0.5/6, 0.2/8}, B = {0.5/2, 0.4/4, 0.1/6, 1/8}
Perform union, intersection, difference, and complement over fuzzy sets A and B.
f) Draw an overview block diagram of a fuzzy system and explain the importance of each of its blocks.
g) Explain Bacterial Foraging Optimization (BFO) algorithm with a flow chart/ step by step algorithm.
h) What are the different bitwise operators used in genetic algorithms? Explain its significance.

i) Explain the training algorithm of the radial basis function network.

j) What is Karmakar's Algorithm? Explain with an example.

k) Write the steps in Adaline training algorithm.

l) Given that X = {x1, x2, x3} Y = {y1, y2} Z = {z1, z2, z3} and R and S be two relations defined on universal set X x Y and Y x Z respectively. R and S are given as $R = \begin{bmatrix} 0.5 & 0.1 \\ 0.2 & 0.9 \\ 0.8 & 0.6 \end{bmatrix}$ $S = \begin{bmatrix} 0.6 & 0.4 & 0.7 \\ 0.5 & 0.8 & 0.9 \end{bmatrix}$

Find R o S, by max-min composition

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** State Kuhn-Tucker conditions. Use them to minimize f (x, y, z) = $x^2 + y^2 + z^2 + 20x + 10y$, subject to $x \geq 40$, $x + y \geq 80$, $x + y + z \geq 120$. **(10)**

b) Write the standard (canonical) form of the following LPP **(6)**
Maximize: $Z = 2x_1 + 3x_2 - 2x_3$, subject to $x_1 + 5x_2 - x_3 \leq 15$, $2x_1 - x_2 + x_3 \leq -10$, $x_1 + 2x_3 = 10$, $x_1, x_2 \geq 0$, x_3 unrestricted in sign

Q4 **a)** What is Fuzzy Inference System (FIS)? With block diagram, explain the working principle of an FIS. Differentiate between Mamdani and Sugeno FIS. **(8)**

b) What is Defuzzification? Explain different types of Defuzzification methods with example. **(8)**

Q5 **a)** What is crossover operator? Discuss different types of crossover operators with example in each case. What is mutation operator? Discuss different types of mutation operators with example in each case. **(10)**

b) What do you understand by 'Tournament Selection' with reference to GA? How does it overcome the demerits of roulette wheel selection? **(6)**

Q6 **a)** Explain the 'back propagation' algorithm in a feedforward neural network with one hidden layer. Derive the relevant expressions. What do you mean by an 'epoch'? **(10)**

b) What is Learning of ANN? What are the different types of learning methods used? **(6)**

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Total Number of Pages: 02 **Course: M.Tech**

Sub_Code: P1PGCC02

1st Semester Regular/Back Examination: 2023-24

SUBJECT: Internet of Things

BRANCH(S): All

Time: 3 Hour

Max Marks: 100

Q.Code : N531

Answer Question No.1 (Part-1) which is compulsory, any eight from Part-II and any two from Part-III.

The figures in the right hand margin indicate marks.

Part-I

Q1 **Answer the following questions:** **(2 x 10)**

a) Differentiate between 6LOWPAN and IEEE 802.15.4-LR WPAN.

b) The huge numbers of devices connected to the IoTs have to communicate automatically, not via humans. What is this called?
(i) Machine to Machine (ii) Bot to Bot (iii) Skynet (iv) Intercloud

c) What are the differences between machines in M2M and things in IoT?

d) _____ is the internet protocol whose another name is WiFi.
(i) 6LoWPAN (ii) IEEE 802.11 (iii) IEEE 802.15.4 (iv) WiMax

e) What are the architectural constraints of REST?

f) What is web service? What are different types of web services used in IOT?

g) Why do IoT systems have to be self-adapting and self-configuring?

h) Differentiate between physical entity and virtual entity in IoT system.

i) What do you mean by data visualization? Explain it

j) What is big-data and why we are using big-data in IOT?

Part-II

Q2 **Only Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 × 8)**

a) Discuss about agility in IOT.

b) What is the IoT framework? Discuss any one of the IoT frameworks with its features.

c) Discuss the following capabilities in an IoT data platform:
- Connectivity - Actionable data - Device management

d) Write the procedure for association request reception and association response reception. How do the nodes decide to become part of the same cluster?

e) What is IoT middleware? Explain MTC/M2M middleware with a neat sketch diagram.

f) Explain the following terms in the context of the identification of IoT objects and services: - Object IDs - Radio-frequency identification - Uniform resource identifier.

g) What are 5-any in the context of device intelligence? What is the role of device intelligence in order to make IoT a reality? Explain.

h) What is Industry 4.0? What are the main characteristics? Discuss various challenges and solutions of Industry 4.0.

i) How to use big data and visualization in IoT? How IoT is driving Big Data?

j) Draw the block diagram of the RFID reader and explain its operation.

k) Explain the hadoop file structure.

l) Explain wireless sensor networks architecture with a suitable diagram.

Part-III

Only Long Answer Type Questions (Answer Any Two out of Four)

Q3 Discuss the security challenges of the EPC global architecture framework with a neat diagram. **(16)**

Q4 What is cloud computing? How Grid, SOA, IoT and cloud are related? **(16)**

Q5 What are the different layers of IoT protocols? Explain functions of all the layers. **(16)**

Q6 What is a software agent? How it is related to IoT? Why does software agents have to be persistent and goal-oriented? **(16)**